LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to semiconductor storage devices, and more particularly to low cost memory resulting from manufacturing efficiencies which construct the devices in three-dimensions and which incorporate efficient testing mechanisms.

Description of Prior Art

Many versions of three-dimensional memory arrays have been disclosed in the prior art and they might be classified as being one of two types - stacked chips and layered manufacture.

Layered approaches are discussed in U.S. Patents 4,525,921, 4,646,128, and 5,432,729 wherein Carson disclosed a technique for bonding two or more memory chips one on top another to form a three-dimensional memory array. There have been variations on this design, such as by Kato in U.S. Patent 5,051,865, in which he discloses an enhancement comprising heat sink layers which are bonded between memory circuit layers to help reduce overheating.

Of greater interest to the present invention, Zhang, in his U.S. Patent 5,835,396, discloses an approach for manufacturing a layered memory device based on diode storage devices at the intersections of the rows and columns within each layer and Rosner, in his U.S. Patent 4,442,507, discloses an electrically programmable read-only memory. Both of these devices are manufactured upon a semiconductor substrate having decoding logic for the associated bit lines of the memory layers.

However, all of these devices have shortcomings. The bonding of multiple chips creates many points of failure and has high associated assembly costs. Manufacturing devices in layers as disclosed in the prior art has the high cost of the base substrate and its electronic circuitry (manufactured using traditional semiconductor manufacturing means) and its associated complexity as well as the many potential points of failure of interconnecting the vast number of row and column bit lines of the various layers.

What is needed is a three-dimensional memory device which can retain the advantage of lower cost manufacturing by not requiring a

base layer comprising the bit line decoding circuitry and the high reliability of few layer interconnects. The present invention accomplishes this by including the decoding circuitry on each memory layer thereby eliminating the need for a base layer comprising bit line decoding circuitry and thereby dramatically reducing the number of layer interconnects to just power and a few address and data lines.

SUMMARY OF THE INVENTION

As advances continue to be made in the area of high density semiconductor storage, the need to keep the cost of these devices low is critical for many applications. Many storage solutions, such as FLASH memory (a non-volatile, rewritable memory technology), are currently very expensive. As a result, many users of FLASH memory must upload and download the contents of their memory to other storage means, such as a computer with a hard disk. This is because FLASH is so expensive that rather than have many FLASH memory devices, users will typically own very few FLASH memory devices which they will reuse depending on their current needs.

The present invention is a means for constructing a high density rectifier matrices (as might be used to construct electronic memory) such that the costs are kept low. By constructing memory devices in three dimensions and integrating simple test circuitry that can rapidly verify the operation of such devices, storage densities can be made very high while keeping testing time (and the associated costs of testing) very low. It is believed that memory devices can be manufactured which will be dramatically lower cost than current technologies.

The present invention also offers advantages over existing technology in that this memory technology could be added to a variety of existing semiconductor devices. Also, a one time programmable variation of the device could be created with little additional effort.

Finally, the present invention also offers advantages over existing technology in that this memory technology, by virtue of its exceptionally simple design, will retain its cost savings even when manufactured three-dimensionally in layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig 1. Illustrates a prepared substrate for the present invention.

Fig 2. Illustrates a front and side view after etching rows.

Fig 3. Illustrates a front and side view of the rows following a passivation step.

Fig 4. Illustrates a front and side view of the passivated rows following etching to open contacts through the passivation layer.

Fig 5. Illustrates a front and side view of the device following final metalization and etching to create columns.

Fig 6. Illustrates a second layer of the device having been manufactured upon a first layer of the device.

Fig 7. Illustrates an interconnection pattern for quick testing of the device.

CROSS REFERENCE TO RELATED PROVISIONAL APPLICATION

The present patent application claims priority to provisional patent application 60/213,419 titled "LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY" which was filed on June 22, 2000 and which is hereby incorporated by reference.

CROSS-REFERENCE TO RELATED PATENTS

This application makes references to U.S. Patent Number 5,889,694 for a "Dual-Addressed Rectifier Storage Device" issued March 1999, to U.S. Patent Number 3,245,051 for "Information Storage Matrices" issued April 1996, and those patents are hereby incorporated herein by reference.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is a means for fabricating semiconductor memory in three dimensions. This memory will be fabricated using a process similar to that used to construct Thin Film Transistor (TFT) flat panel displays - in particular, using deposited semiconductor material on insulating substrates.

Refer now to the figures which show a preferred embodiment of the invention. Figure 1 shows a possible configuration of a prepared substrate. This substrate consists of a base (1) that is typically made of glass, of Silicon Dioxide on a silicon wafer, or of other insulating material. On top of this is deposited about 1000 Å of metal (2) such as TiAu (Ti-gold), Ni (Nickel), or Al (Aluminum). Next is deposited 250 Å of N+ amorphous Silicon (N+ αSi:H) (3) followed by 1000 Å of αSi:H (4). Finally, 100 Å of metal (5) is deposited. It should be noted that the metals and the thicknesses are not critical, so long as certain functional requirements are met. Bottom metal (2) can be made of any material that will form an ohmic contact with the layer (3) above it. Bottom metal (2) should be thick enough to carry enough current to provide the operational speed desired given any circuit capacitances. Layer (4) can be one of many materials that will form an ohmic connection between layers (2) and (4) and need only be thick enough to prevent layers (2) and (4) from interacting in a non-linear way (i.e., not a rectifying contact). Layer (4) can be one of many materials that will form a rectifying contact with top metal layer (5) and need only be thick enough to allow for an adequate junction depth for proper operation of that rectifying contact. Top metal (5) can be made of any material that will form a rectifying contact with the layer (4) below it

and need not be very thick because additional metal will be deposited directly on top of this in a later step. Finally, all thicknesses must be thin enough to not create unacceptable aspect ratios (i.e., very tall, thin rows that are too tall for their widths), given the design feature size, when these layers are etched as described below.

Figure 2 shows the device following etching steps that result in many parallel rows having many “towers” of rectifiers on each of them. The width of these rows must be proportional to the thickness of the substrate layers so that the aspect ratio are manageable; if the rows or towers are too tall, given their footprints, they will fall over. The width of the channels between the rows and towers must be wide enough to minimize interaction of adjacent rows and columns.

Figure 3 shows the rows following passivation - that is to say, the channels between the rows and columns are filled in with insulating material (6) for structural strength, to provide a smooth surface for subsequent photolithography steps, and to insulate the sides of the rows and columns from the deposition of the top metal layer for the column connections.

Figure 4 shows the array following an etch to create openings to the towers through insulating material (6). These openings are made selectively in order to program the device according to U.S. Patent 5,889,694. Note that the thickness of the passivated material on top of those towers where no opening is etched must be sufficient to ensure electrical insulation from the top metal layer (yet to be deposited). It should also be noted that all data bit connections could be opened in the case of a programmable or writable device. Such a programmable device might have an additional layer or might otherwise provide for a fusable or antifusable link in each of the towers used for data storage. This additional layer might also be made of a thin-film material that is a phase-change chalcogenide alloy similar to the film used to store information on commercial CD-RW and DVD-RAM optical disks. Note that some of the etches go all the way down to the bottom metal layer (2) to enable the formation of direct connections to the bottom metal rows. Steps 3 and 4 can be partly combined by using a photosensitive spin-on insulator, such as Polyimide, which can be deposited and then photolithographically patterned and developed.

Figure 5 shows the final device following the deposition of top metal layer (7) and the etching of that layer into columns orthagonal to the rows. The result of this process will result in a 2 dimensional array of rectifying contacts (in this case, schottky diodes). The rows

will be connected by the top Metal 3 layer and the columns will be connected by the bottom Metal 1 layer. This top layer is expected to be about 2000 Å thick, but should be thick enough to carry enough current to provide the operational speed desired given any circuit capacitances without creating any of the previously mentioned aspect ratio problems when the columns are etched.

It is believed that the simplest construction would be as described above utilizing schottky type rectifying contacts. However, many other rectifying structures could be used; the bottom metal layer (2) and top metal contact (5) could be ohmic and the junction between layers (3) and (4) could form the rectifying contact. For example, if layer (3) was doped N+ and layer (4) was doped P+, a P-N rectifying junction could be formed. Alternatively, some other semiconducting material, such as an organic molecule, could be used in place of amorphous silicon. Another variation could include multiple rectifying junctions in series. This might be achieved by constructing a P-N junction and a schottky junction. With this multiple stacked rectifying towers design, if one of the rectifying devices was defective and formed an ohmic connection instead of a rectifying connection, the others in the series would result in the tower still being a rectifying connection between the top column and the bottom row as required for such a rectifier storage matrix.

Figure 6 shows the result of this process if repeated on a substrate which has already had this process performed once. Note that the first layer will most likely be planarized with a polishing step before depositing an insulating film to start the second layer. In the case of the DRS memory constructed in multiple layers, these layers can be wired mostly in parallel (as described in U.S. Patent 5,889,694), only the bonding pads would be interconnected by vias. As can be seen, the structure is identical except for the inclusion of vias (8) to interconnect the bonding points for power, ground and the complementary address inputs of each layer. The data bonding pads would be brought to the surface layer independently so that each data bonding pad would connect to a single layer. Other configurations of wiring are possible. For example, if the data lines of each layer were interconnected by vias and separation was instead accomplished by having some address lines connected to specific layers so as to in effect enable only a single layer at a time and thereby multiplex the data connections. This would be the equivalent of implementing the selective powering of the device as is disclosed in U.S. Patent 5,889,694 whereby each individually powered section of the device was comprised in a separate layer.

Figure 7 shows an interconnection technique for the rows (and would be repeated for the columns) to enable the quick and inexpensive testing of the device. The most common faults expected to occur during the fabrication of the present invention are breaks in a line or shorts between two adjacent lines. With the present interconnection technique, all the alternate rows are connected end to end with a top layer connection thereby creating two conductive snakes - one comprising all the even numbered rows (9) and the other comprising all the odd numbered rows (10). By doing so, one can test the device by probing the two ends of each snake and checking for continuity. This will enable instantaneously checking the all the rows for any breaks with just four probe points. Also, shorts between rows can be identified simultaneously by checking for any continuity between the two snakes. The columns would be simultaneously checked in an identical fashion. Also, in the same way and at the same time, the device can be checked for shorts between the top columns and bottom rows (taking care to select one range of voltage levels for the rows and another range of voltage levels for the columns such that the diodes are reverse biased). By combining this test technique with the multiple stacked rectifying towers design, if a device passes this instantaneous test, one can be highly confident of having a working device. After identifying any defective devices (which, if the devices are manufactured inexpensively enough, would most likely just be marked to be discarded), these top layer connections are etched away to separate the lines or the edges of the chips where the interconnections are found could be cut back just enough to remove those edges and their interconnections.

This process is initiated by depositing layers on an insulating substrate such as plastic or glass. But, it should be noted that this insulating substrate does not have to be limited to plastic or glass. As has been shown in the prior art, this process could be performed on top of a normally fabricated semiconductor device such as a memory controller chip, an error detection and correction chip, a data decryption (and, optionally, encryption) chip (such as for security like DES or PGP or for storage efficiency like MP3), or a microprocessor, or the like that has been passivated with a top layer of protecting glass or other insulator. An array of LEDs or diode optical sensors might be constructed upon an image processor to construct a micro display or camera. In its simplest form, a diode matrix (such as was disclosed by Robb in his U.S. Patent 3,245,051, issued in 1965) could be constructed on top of a memory controller comprising the address decoding, the row and column selection logic, the line driver-amplifiers, and the sense

amplifiers; in this case, the individual connections to the rows and columns would be made up from the controller substrate. Since a storage array could cover a greater area then, say, a memory controller chip, multiple memory controllers could be placed on the chip to be covered according to the present invention thereby providing redundant controller circuits to operate the storage array, resulting in higher fabrication yields. Furthermore, this process can be performed on top of itself resulting in a three-dimensional construction of this memory device with many layers. One would only then simply have to interconnect the two or more layers with vertical via connections. In the case of the DRS memory constructed in multiple layers, these layers can be wired mostly in parallel; just as the DRS array can be divided into multiple areas on one layer (as described in U.S. Patent 5,889,694), these multiple areas could be constructed vertically with this technique.

Other variations would include the fabrication of integrated memory circuits using other than traditional photolithographic semiconductor manufacturing techniques. By combining lower cost manufacturing techniques with the higher densities resulting from three-dimensional fabrication, the cost per bit can be driven even lower.

The foregoing description of an example of the preferred embodiment of the invention and the variations thereon have been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by any claims appended hereto.